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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,596	03/15/2004	Motoyasu Yano	SON-2959	8282

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EXAMINER	
CHAN, EMILY Y	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-D

Office Action Summary	Application No.	Applicant(s)	
	10/799,596	YANO ET AL.	
	Examiner	Art Unit	
	Emily Y. Chan	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7-9 and 11-13* is/are rejected.

7)☒ Claim(s) *2-6 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some* c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: "detect detection " found in pages 16 and 17 should be "defect detection".

Appropriate correction is required.

Claim Objections

Claims 1,7 and 8 are objected to because of the following informalities: the recitation " the input of a signal indicating a defect detection mode " lacks antecedent basis because in the claims, it is never recited when and how the image display device goes to the defect mode. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 7-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brook U S Patent No 3,742356 in view of Devos et al US Publication No. 2005/0017922.

With respect to claims 1 and 7-8, Brook ('356) expressly discloses an apparatus (see Figs 1 and 2) for testing light emitting diodes as claimed comprising:

a plurality of light-emitting diodes (11a, 11b) arranged by a predetermined arrangement on an image display face (10);

a defect detection portion (see Fig. 2) for electrically detecting a defect from said plurality of light-emitting diodes (see Col. 2, lines 52-66).

Brook ('356) also discloses a signal indicating a defect detecting mode (see Col. 2, line 53-54 " responsive to an indication on a "start test" line for initiating the sequencing of the diodes") but fails to disclose a voltage detection portion for applying a constant current to the plurality of light –emitting diode and for detecting a voltage between terminals of a light emitting diode.

Devos et al ('922) disclose an image display device (see Figs.1 and 2) comprising a plurality of light-emitting diodes (212) arranged by a predetermined arrangement on an image display face (210). Devos et al ('922) exclusively teach a voltage detection portion (220) for applying a constant current (214 and see page 3, paragraph (0025)) to said plurality of light-emitting diodes (212) in an off region at a forward voltage or less (when the switch 218 is off) and detecting a voltage between terminals of a light emitting diode arising when the constant current flows there through (see page 3, paragraphs (0029 and 0030)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the voltage detection portion as taught by Devos et al ('922) into Brook ('356)'s system for the expected benefit of overcoming light output variations due to organic light-emitting diode (OLED) aging as disclosed by Devos et al ('922) (see page 1, paragraph (0001)).

With respect to claim 9, Devos et al ('922) disclose that a current source (214) is connected in series with said light-emitting diodes (212) and a predetermined number of

comparators (see page 5, paragraph (0044)) for comparing a voltage of one terminal of a light-emitting diode (212) changing in proportional to said voltages between terminals as a result that said constant current flows in said current source with an input reference voltage ("predetermined minimum threshold voltage").

With respect to method claim 11, the recited first, second and third steps can be performed by the references of Brook ('356) in view of Devos et al ('922) (see rejection for apparatus claims 1 and 7-9 above).

2. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brook ('356) in view of Devos et al ('922) as applied to claims 1 and 7-9 above, and further in view of Saito Koichi Japan Publication 04-305173.

Brook ('356) in view of Devos et al ('922) do not specify in the third step to judge the light –emitting diode having a voltage between terminals at a position being away from an end on the low voltage side as a short-circuited defect or a defect with a high probability of becoming short-circuited.

Saito Koichi ('173) discloses a checking circuit for light emitting diode (see abstract) and exclusively teach a method for electrically detecting and judging a defect from said plurality of light-emitting diodes to be a "short-circuited diode" based on the result of a voltage corresponding to the min. value with the reference voltage comparison (see CONSTITUSION).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the teaching of Saito Koichi ('173) into Brook ('356) in view of Devos et al ('922)'s system for the expected benefit of

automatically check the normality of the light emitting diode even when the diode is visually confirmed by a person as disclosed by Saito Koichi ('173) (see PURPOSE).

Allowable Subject Matter

3. Claims 2-6 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 2-6 and 10 are indicated allowable because the prior art in the record does not teach or suggest a device for testing defect of light-emitting diode with detail of all the elements in combination recited in the claims 2-6 and 10. Specifically, the prior art does not teach that the voltage detection portion comprises a plurality of drive circuits connected in series in one direction for respectively driving a predetermined number of the light-emitting diode and the defect detection portion transfers data and detects the defect in every horizontal direction recited in claim 2. Claims 3-6 are dependent on claim 2 and are indicted allowable accordingly. The prior art also does not disclose or suggest a logic calculation unit on outputs of said predetermined number of comparators and a transfer register for adding binary data output from said logic calculation unit recited in claim 10.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kamata et al US Patent NO. 4,346,347 disclose a diode fault detecting apparatus.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y. Chan whose telephone number is 571-272-1956. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC
8-16-05

Jermele Hollington
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AU 2829
08/19/05